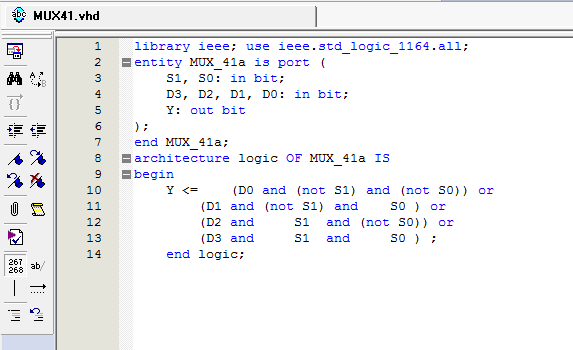
Lab 6 Summary

Irvin, Mitchell

Section 7441

3/11/16

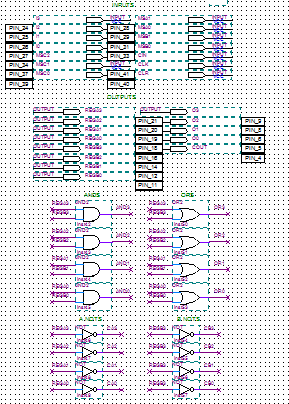
Prelab Part 1: VHDL of a 41MUX



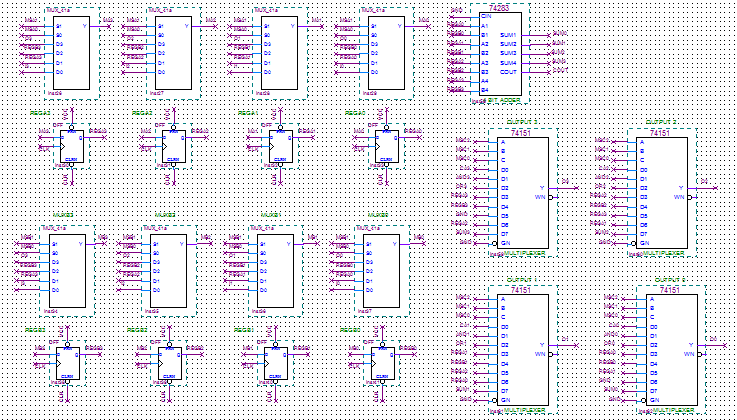
Verify that it works: if it didn’t work the rest of my lab wouldn’t work. I compiled it and created a VWF file to test it but that entire project folder got corrupted and I had to redo everything so please just let the rest of my lab be proof that it works

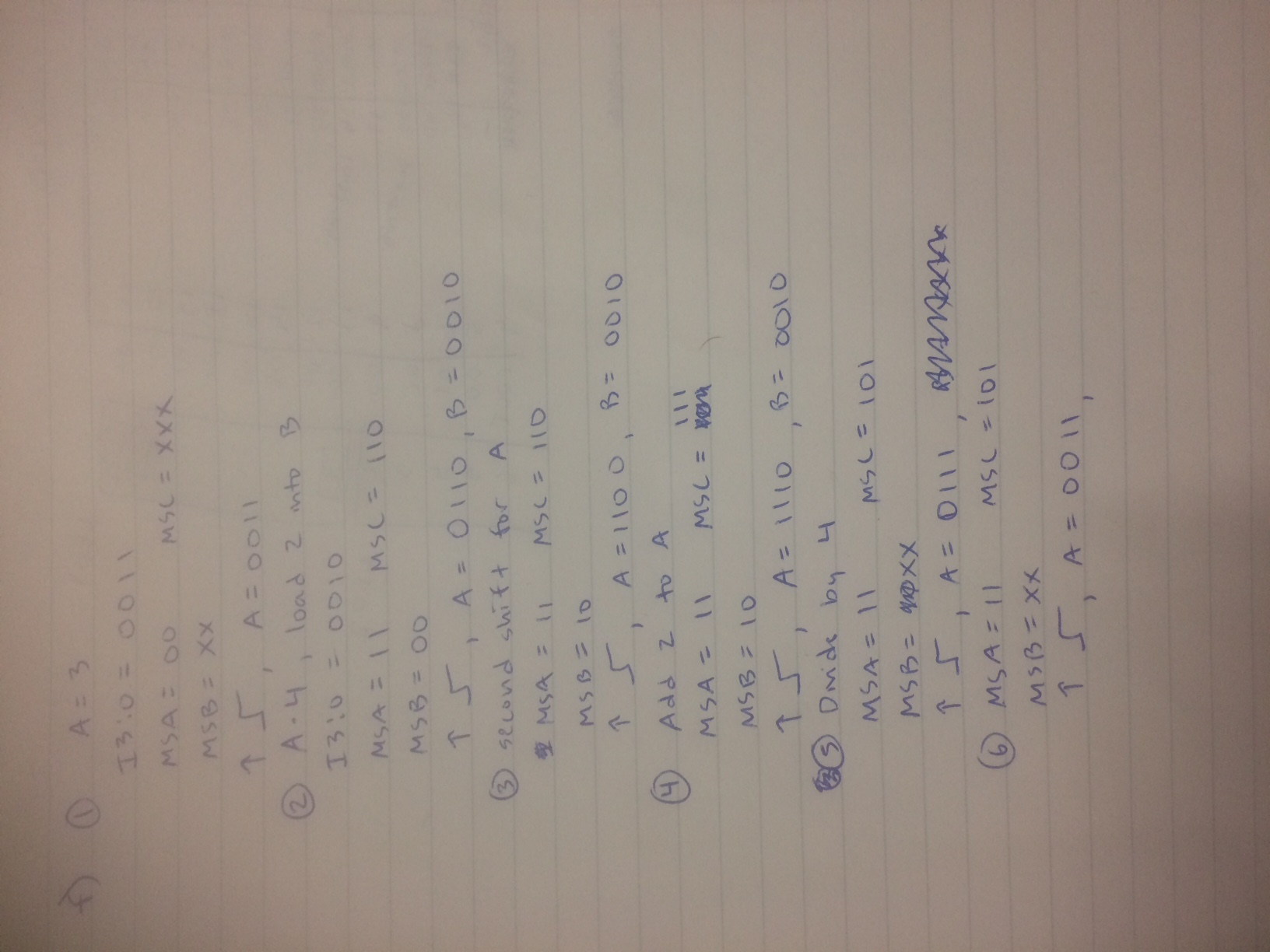
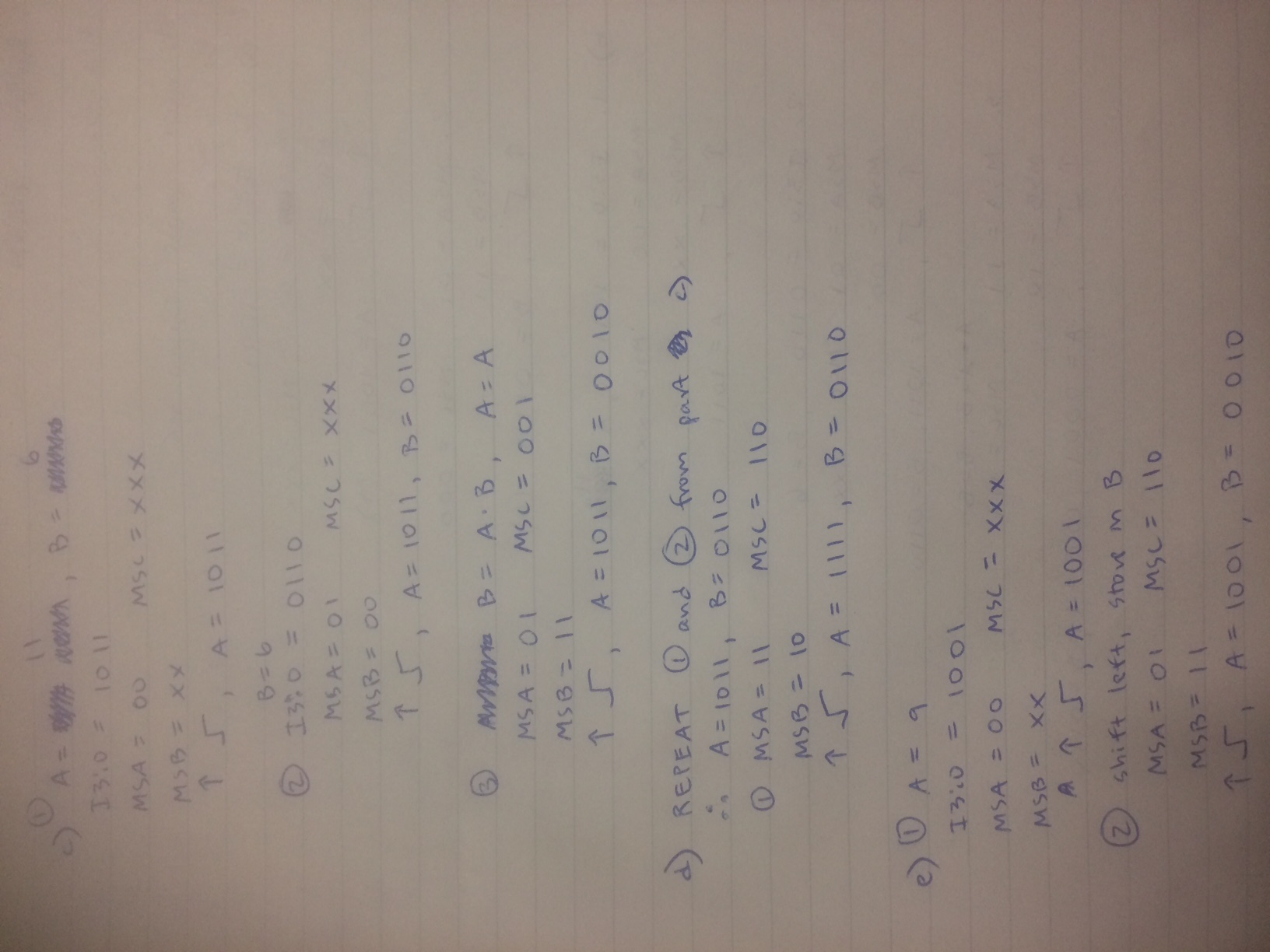
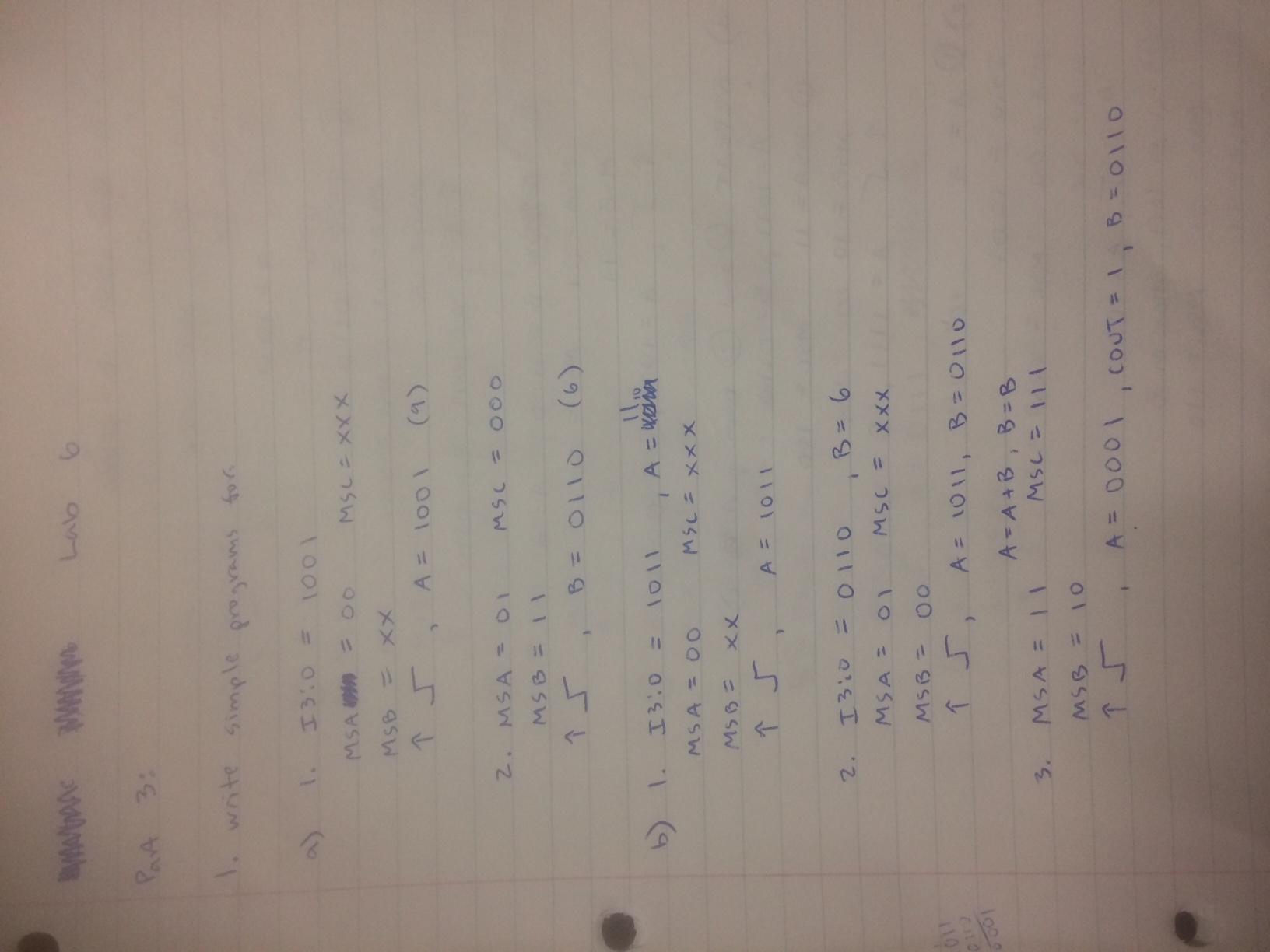
Part 2: ALU Design

Inputs/Outputs



Logic Design



Part 3: Simple Program Design

Verification of Prelab Part 3 in Quartus

